

5 What is claimed is:

1 1. A process, comprising:

2 forming a first dielectric layer on a substrate;

3 patterning the first dielectric layer such that a plurality of vertically

4 oriented posts are formed, the post having a top surface;

5 forming a second dielectric layer over and adjacent to the posts, the

6 second dielectric layer having a top surface; and

7 polishing the second dielectric layer such that its top surface is

8 substantially even with the top surfaces of the posts.

1 2. The process of Claim 1, wherein the substrate comprises a dielectric

2 material.

1 3. The process of Claim 1, wherein the substrate is a material selected from

2 the group consisting of silicon carbide, silicon nitride, and carbon doped oxides of

3 silicon.

1 4. The process of Claim 1, further comprising curing the second dielectric

2 layer.

1 5. The process of Claim 1, further comprising aging the second dielectric

2 layer.

1 6. The process of Claim 1, further comprising forming dual damascene

2 openings in the second dielectric layer.

1 7. The process of Claim 1, wherein forming the first dielectric layer
2 comprises depositing an oxide of silicon.

1 8. The process of Claim 7, wherein forming the second dielectric layer
2 comprises chemical vapor deposition of a low-k material.

1 9. The process of Claim 7, wherein forming the second dielectric layer
2 comprises spinning on a low-k material.

1 10. The process of Claim 1, wherein the second dielectric has a lower
2 dielectric constant than the first dielectric.

1 11. A dielectric structure, comprising:
2 a plurality of posts disposed on a substrate, the posts comprising an
3 electrically non-conductive material; and
4 a low-k dielectric material disposed around the posts.

1 12. The dielectric structure of Claim 11, wherein the substrate comprises a
2 material selected from the group consisting of silicon carbide, silicon nitride, and
3 carbon doped oxides of silicon.

1 13. The dielectric structure of Claim 11, wherein the posts are vertically
2 oriented and comprised of an oxide of silicon.

1 14. The dielectric structure of Claim 13, wherein the oxide of silicon is a
2 fluorine doped oxide.

1 15. The dielectric structure of Claim 13, wherein the posts have a rectangular
2 base.

1 16. An integrated circuit, comprising:
2 a substrate having interconnected electrical elements therein;
3 a first dielectric layer disposed over the substrate;
4 at least one electrically non-conductive, vertically oriented post disposed
5 on the first dielectric layer; and
6 a second dielectric layer disposed on the first dielectric layer such that the
7 second dielectric surrounds the at least one post.

1 17. The integrated circuit of Claim 16, wherein the second dielectric layers has
2 trenches therein.

1 18. The integrated circuit of Claim 17, further comprising metal disposed in the
2 trenches.

1 19. The integrated circuit of Claim 18, wherein the metal comprises copper.

1 20. An integrated circuit, comprising:

2 a substrate having interconnected electrical elements therein;

3 a first dielectric layer disposed over the substrate;

4 a plurality of electrically insulating structures disposed on the first dielectric
5 layer; and

6 a second dielectric layer disposed on the first dielectric layer such that the
7 second dielectric surrounds the plurality of structures.

1 21. The integrated circuit of Claim 20, wherein the structures are identical.

1 22. The integrated circuit of Claim 20, further comprising metal filled
2 damascene trenches in the second dielectric layer.

1 23. The integrated circuit of Claim 20, wherein the structures are comprised of
2 an oxide of silicon, and the second dielectric layer is comprised of a porous
3 material having a dielectric constant lower than that of silicon dioxide.

24. A process, comprising:
2 depositing a silicon nitride layer on a wafer;
3 depositing an insulating layer over the silicon nitride layer;
4 patterning the insulating layer such that a plurality of structures are

5 formed, the structures each having a top surface;
6 depositing a porous dielectric material over and adjacent to the
7 structures, the porous dielectric material having a void fraction; and
8 polishing the porous dielectric material such that a top surface thereof
9 is substantially even with the top surfaces of the structures;
10 treating the porous dielectric material such that its void fraction is
11 increased.

1 25. The integrated circuit of Claim 24, wherein the porous dielectric material
2 has a lower dielectric constant than that of the structures.

*Added
C27*

007227 50454250